The DØ Run 2b Silicon Microstrip Tracker

APS Meeting
April 5-8, 2003

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Outline

- Run 2B upgrade goals
- Why a new Silicon Detector?
- Expected performance
- Detector design
- Summary

Run 2B upgrade goals

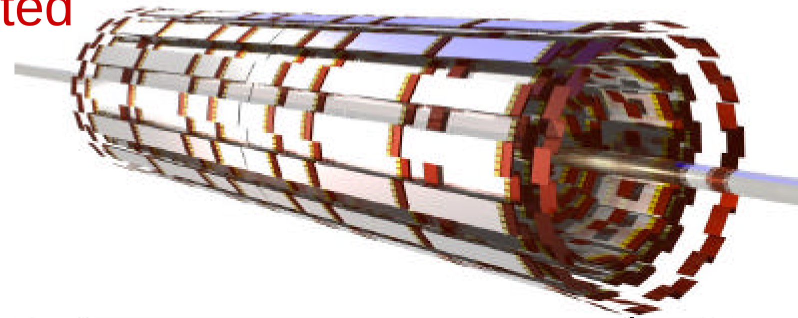
- There is a single Run 2 program that evolves as a function of Luminosity
  - Confront the standard model through precise measurements (strong interaction, quark mixing matrix, EW force, top quark…)
  - Direct search for particles and forces not yet known (Higgs, SUSY…)
- The goal of the Run 2B upgrade is to maximize this program exploiting the full potential of the Tevatron
  - Higgs observation (114 < M_H < 190 GeV)
  - Top mass and properties, single Top production
  - W/Z improved measurements (M_W, effective $\sin^2\theta_W$ to 0.0002,…)
  - Test QCD itself, better understanding of backgrounds
  - SUSY signatures

Why a New Silicon Detector?

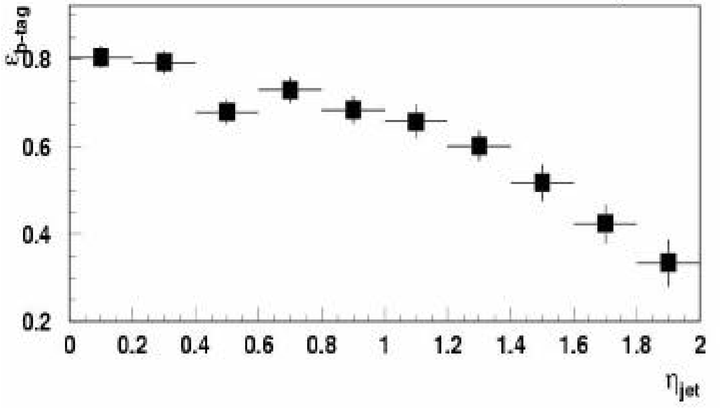
- Current DØ silicon tracker was built to withstand 2-4 fb^{-1} of Integrated Luminosity
- Extended Run2 with higher Luminosity (~10 fb^{-1} achievable)
  - Increase in integrated luminosity
    - Depletion voltage will exceed breakdown voltage after 2 - 4 fb^{-1} for innermost layers.
  - Increase in instantaneous luminosity
    - Need of better pattern recognition (more layers of silicon)
    - Trigger upgrades
- Guiding Principles
  - Minimal cost
  - Full replacement, minimum shutdown time
  - Design *must* allow for assembly to be ready in 3 years

Performance of Proposed Detector

- Performance studies based on full GEANT simulation
  - Full model of geometry and material
  - Model of noise, mean of 2.1 ADC counts (2000 e^-, S/N~12)
  - Pattern recognition and track reconstruction
  - Longitudinal segmentation implemented
  - Single hit resolution of ~11 μm

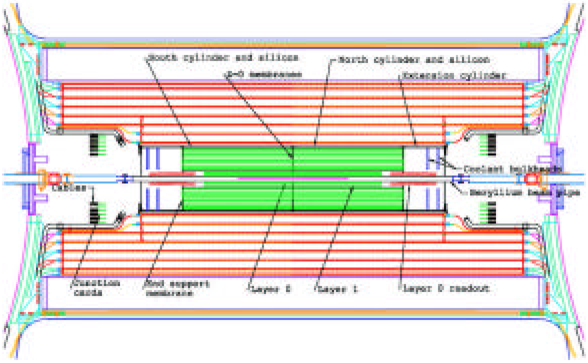


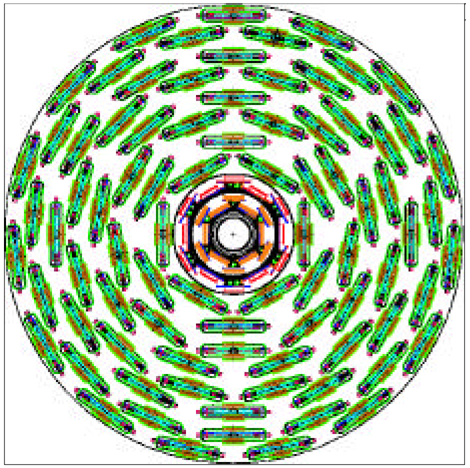
- Benchmarks
  - $\sigma(p_T)/P_T$ ~ 3% at 10 GeV/c
  - $\sigma(d_0) < 15\ \mu$m for $p_T > 10$ GeV/c
- b-tagging
  - b-tagging efficiency of ~ 65% per jet



Detector Design

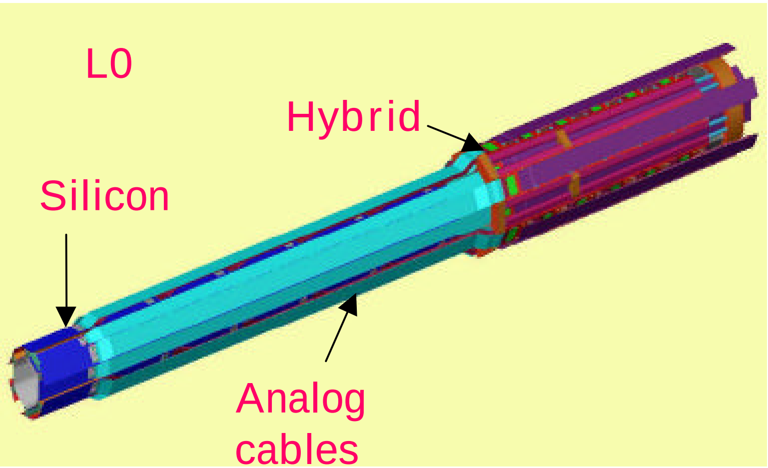
- Employ single sided silicon
  - Must be radiation-hard (up to 15 MRad)
- Six layer silicon tracker
  - 18mm < R < 164mm
  - Divided in two groups
- Spatial Considerations
  - Installation within existing fiber tracker
  - Full tracking coverage
    - Fiber tracker up to $|\eta| < 1.6$
    - Silicon stand-alone up to $|\eta| < 2.0$
- No element supported from the beam pipe
- Data Acquisition and Silicon Track Trigger
  - Retain readout system outside of calorimeter
  - Total number of readout modules cannot exceed 912

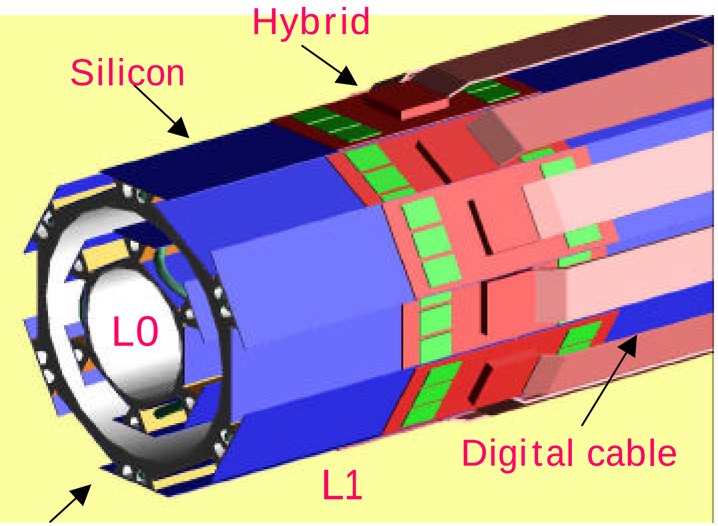




Layers 0 and 1

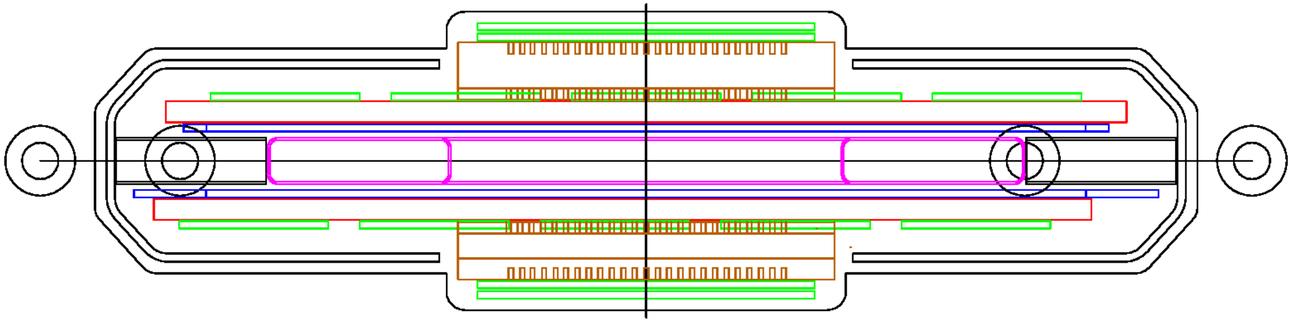
- Tight space, not supported by beam tube
- Minimize material
- Cool to -10 ^{o}C to increase sensor lifetime (T< -5 ^{0}C for Layer1)
- Readout electronics:
  - No hybrids mounted on sensors for L0: analogue cables
  - Mounted on Silicon in Layer 1





Layers 2-5: Staves

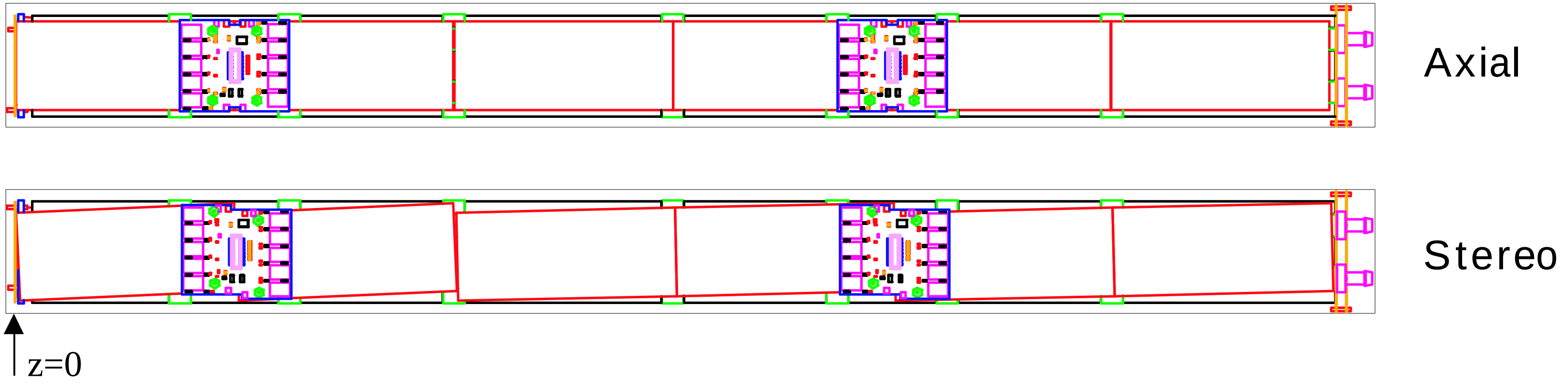
- Basic building block of the outer layers is a stave



- Stave is:
  - two-layer structure of silicon sensors
  - One layer of axial only, and one layer of stereo only readout
  - Total of 168 staves
- C-shells at edge of stave provide stiffness
- Staves are positioned and supported in carbon fiber bulkheads at z = 0 and z = 605 mm.
  - Locating features on stave provide the alignment

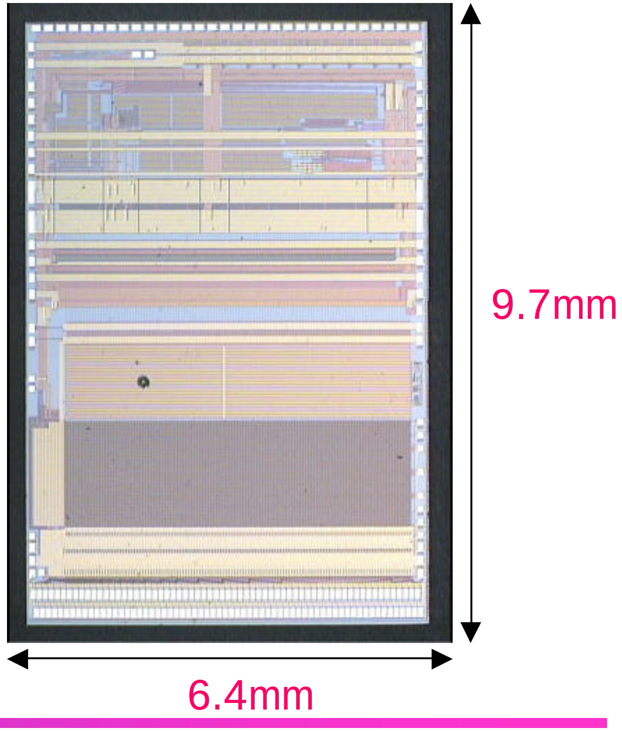
Readout Modules (Layers 2-5)

- Each stave has four readout modules
- Readout module length varies with z-position.
  - For all layers, the modules closest to z = 0 are 200 mm long
  - Those furthest from z = 0 are 400 mm long
- Four Readout module types
  - 10-10 (axial, stereo)
  - 20-20 (axial, stereo)
  - Ganged sensors will have traces aligned (sensors are 10cm long)
- Module configuration



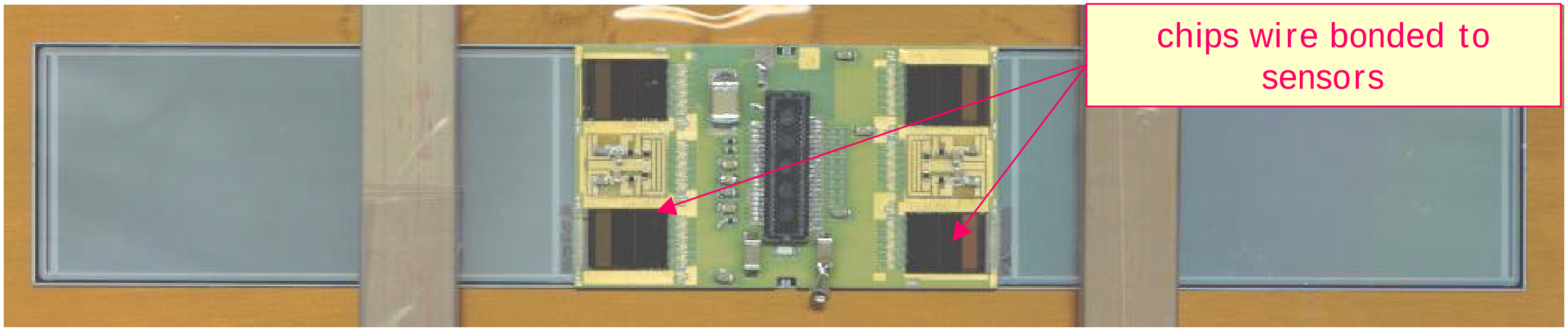
SVX4 Chip

- Some SVX4 characteristics
  - 0.25 μm technology, intrinsically rad-hard (>30Mrad)
  - Successor of SVX2 and SVX3 chip
  - Major success in commonality between CDF and DØ
  - 128 inputs and 47 pipeline cells
  - 8-bit ADC with sparsification /channel
  - 53 MHz readout, 106 MHz digitization
  - ~ 100,000 transistors
  - Programmable test pattern, ADC ramp, preamp bandwidth, calibration, polarity…

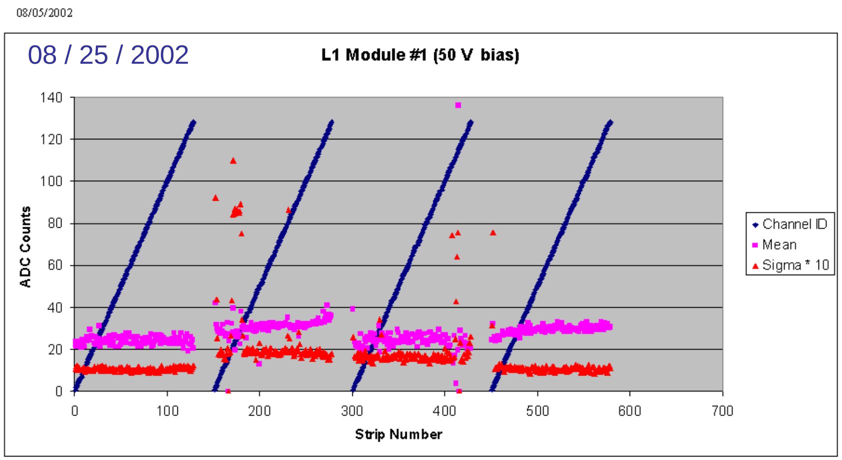


Working Layer1 prototype

- Hybrid mounted on two Layer 1 sensors



- Sigma of pedestal
  ~ 1 ADC count (no sensor)
  ~ 1.8 ADC counts w/ sensor
  (1ADC~900e$^-$)
- Signal/Noise ~ 12/1



Summary

- A lean and robust Silicon Tracker has been designed to pursue the physics goals for Run IIB
- Potential for Higgs observation in Run2 at Fermilab
- Improvement in crucial measurements
  - Top, Electroweak, QCD backgrounds, SUSY signatures…
- The upgraded tracker will ensure
  - Efficient tracking in a high occupancy environment
  - Efficient tagging of heavy flavor jets
- The project has already fully working electrical modules with SVX4 readout
- Moving beyond the prototyping stage